AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): An information processing apparatus comprising:

first and second computer elements which execute the same instructions substantially simultaneously in substantial synchronism, and which have first and second memory elements, respectively, wherein said first and second memory store first and second data, respectively;

a monitor element which finds which of said computer elements is out of said synchronism;

a third memory element which stores an address ~~accessing a data word~~ directed by a write access request at the time when said monitor element finds that said first computer element is out of said synchronism and thereafter; and

a copy element which copies third data associated with said address or addresses out of said second data stored in said second memory to said first memory element when said monitor element finds that said first computer element is out of said synchronism

wherein said monitor element is connected to a bus which is directly connected to a processor of said first and second computer elements;

wherein said monitor element receives address strobes from said processor during the same cycle in order to determine whether said first computer element is out of said synchronism.

2. (original): The information processing apparatus as claimed in claim 1, wherein said copy element is activated unless a permanent failure occurred in said first computer element.

3. (original): The information processing apparatus as claimed in claim 1, wherein said monitor element finds that said first computer element is out of said synchronism based on the time in which it receives first signals from all of said computer modules.

4. (original): The information processing apparatus as claimed in claim 1, wherein said monitor element finds that said first computer element is out of said synchronism based on the time, commands and addresses of requests from all of said computer modules.

5 - 8 (canceled).

9. (previously presented): The information processing apparatus as claimed in claim 1, wherein said third memory element stores an address or addresses which is directed when contents of a cache is written to said memory element.

10. (previously presented): The information processing apparatus as claimed in claim 1, wherein said address indicates the location in said first memory which has possibility of inconsistency with said second memory.

11. (original): The information processing apparatus as claimed in claim 1, wherein said copy element copies said part of the data by utilizing a direct memory transmission.

12. (currently amended): An information processing apparatus comprising:

first and second computer elements which execute the same instructions substantially simultaneously in substantial synchronism, which have first and second memory elements, respectively, and each of which has at least one processor and a bus connected to said processor, wherein said first and second memory store first and second data, respectively;

a monitor element which is connected to said bus and which finds which of said computer elements is out of said synchronism;

a third memory element which an address ~~accessing a data word~~ directed by a write access request at the time when said monitor element finds that said first computer element is out of said synchronism and thereafter; and

a copy element which copies third data associated with said address or addresses out of said second data stored in said second memory to said first memory element when said monitor element finds that said first computer element is out of said synchronism;

wherein said monitor element receives address strobes from said processor during the same cycle in order to determine whether said first computer element is out of said synchronism.

13. (previously presented): The information processing apparatus as claimed in claim 12, wherein said copy element is activated unless a permanent failure occurred in said first computer element.

14. (previously presented): The information processing apparatus as claimed in claim 12, wherein said monitor element finds that said first computer element is out of said synchronism based on the time in which it receives first signals from all of said computer modules.

15. (previously presented): The information processing apparatus as claimed in claim 12, wherein said monitor element finds that said first computer element is out of said synchronism based on the time, commands and addresses of requests from all of said computer modules.

16 - 19 (canceled).

20. (previously presented): The information processing apparatus as claimed in claim 12, wherein said third memory element stores an address or addresses which is directed when contents of a cache is written to said memory element.

21. (previously presented): The information processing apparatus as claimed in claim 12, wherein said address or addresses indicates the location in said first memory which has possibility of inconsistency with said second memory.

22. (previously presented): The information processing apparatus as claimed in claim 12, wherein said copy element copies said third data by utilizing a direct memory transmission.

23. (canceled).

24. (canceled).